Analysis of technological concerns on electrical characteristics of SOI power LUDMOS transistors

G. Toulon[1,2], I. Cortés[1,2], F. Morancho[1,2], E. Hugonnard-Bruyere[3], B. Villard[3] and W. J. Toren[3]
[1]CNRS; LAAS; 7, Avenue du Colonel Roche; F-31077 Toulouse, France
[2]Université de Toulouse; UPS, INSA, INP, ISAE; LAAS; F-31077 Toulouse, France
[3]ATMEL Rousset; Zone Industrielle; 13106 Rousset Cedex, France
e-mail: gtoulon@laas.fr

***Abstract*—This paper is focused on the optimization design of 150 V power LDMOS transistors with the purpose of being integrated in a new generation of Smart-Power technology based upon a 0.18µm SOI-CMOS technology. Different structure parameters, such as the STI length, the N-well doping profile and the relative position of the N-well mask to the STI are analyzed in terms of voltage capability, specific on-state resistance and safe operating area.**

I. INTRODUCTION

The lateral-double-diffused MOS (LDMOS) transistor is the best suited power device for Smart-Power applications thanks to its ease of integration and isolation with submicron CMOS technology [1]. One of the constraints in switching applications is the reduction of the device specific on-state resistance ($R_{on\text{-}sp}$) for a given breakdown voltage (V_{BR}), in order to find the optimal $R_{on\text{-}sp}/V_{BR}$ trade-off. For lithography resolution of 0.25µm and lower, the LOCOS oxidation has evolved to more precise shallow trench isolation (STI) oxidation [2]. The STI assures an improvement of electric field distribution in the drift region, moving further away the harmful electric field from the gate surface edge [3] and lower R_{on} degradation [4] induced by hot-carrier injection. Power LDMOS transistor used as a switch must also survive transitions between on and off states [5]. The boundary of electrical safe operating area (SOA) is linked also with the LDMOS design considerations used to improve the well-known $R_{on\text{-}sp}/V_{BR}$ trade-off, especially those concerning with the channel/STI region definition. Hence, extensive analysis of SOA must be performed in future LDMOS designs for Smart-Power applications in order to optimize both SOA and $R_{on\text{-}sp}/V_{BR}$ trade-off considerations.

II. MEASUREMENT ANALYSIS

A. Structures description

In this section, both P and N-channel power LDMOSFETs on Thin-SOI substrates are extensively analyzed in terms of voltage capability. The schematic cross section of the LDMOS designs envisaged in this study: (a) the simulated N-channel LDMOS structure —also called R-LUDMOS— with the most important design parameters and (b) the SEM image are represented in figure 1.

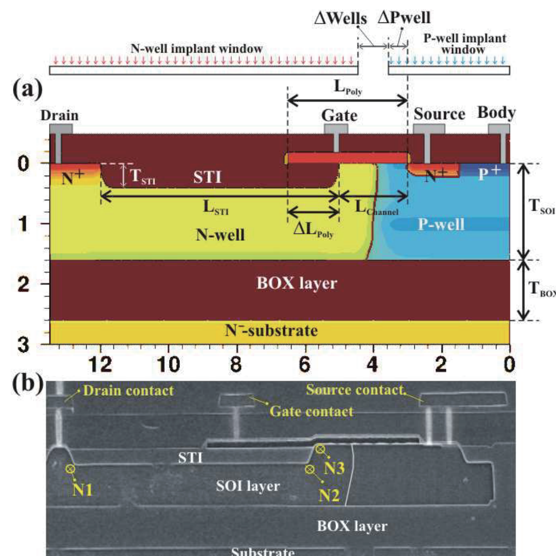

Figure 1. (a) simulated cross section of the R-LUDMOS with all the most important design parameters and (b) SEM image of a fabricated RESURF-LUDMOS transistor.

All the analyzed LUDMOS structures have the same Thin-SOI substrate with a SOI layer (T_{SOI}) and buried oxide (T_{BOX}) thicknesses of 1.6 µm and 1 µm, respectively. The same drift region length (L_{LDD}) of 8 µm for a total cell length (L_{cell}) of 11.5 µm is also considered. The P and N-well regions, which mask positions are defined by ΔWells and ΔPwell parameters (see Figure 1), are defined after the STI formation with high energy multi-ion implantation sequences, including a low energy implantation on the surface in order to adjust the threshold voltage (V_{TH}).

B. Breakdown vs Handle Wafer Voltage evolution

The complete set of the measured electrical characteristics presented in this article are investigated using technological TCAD tools. The breakdown voltage evolution of R-LUDMOS as a function of substrate (handle wafer) voltage (HWV) is represented figure 2 for two different values of ΔWells, which represents the spacing between the P- and N-well masks.

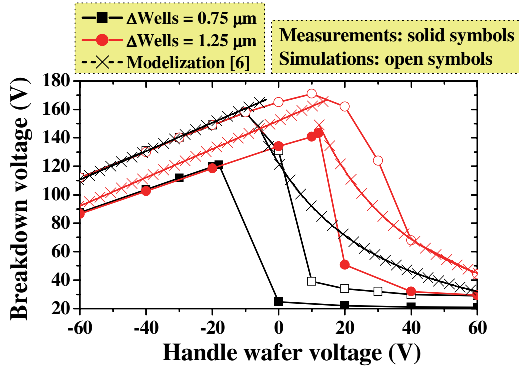

Figure 2. V_{BR} Breakdown voltage as a function of HWV for different ΔWells values. (ΔPwell = 0.75 µm). Measures show smaller V_{BR} due to the LDMOS edge termination definition.

The bell shaped curves on figure 2 can be divided in two regions which define two breakdown localization zones in the drift (LDD) region of the LUDMOS structures [6]. For negative HWV, the drift region is fully depleted and breakdown occurs at the drain side. On the contrary, for positive HWV, the LDD is no longer fully depleted and breakdown is located on source side under the gate electrode. At the limit between the two regions, the maximum breakdown voltage is achieved and electric field is equally distributed between the two regions. For ΔWells of 0.75 µm, the maximum V_{BR} is achieved at negative HWV of -20 V, indicating that the N-well implantation dose exceed the dose for optimal RESURF conditions. For ΔWells of 1.25 µm, the N-well mask position is aligned with the STI edge at the source side, leading to the removal of the Phosphorus implantation in the channel surface, thus giving better V_{BR} evolution conditions. Hence, the ΔWells parameter has an influence on the N-well implanted dose giving the optimal HWV as seen figure 3.

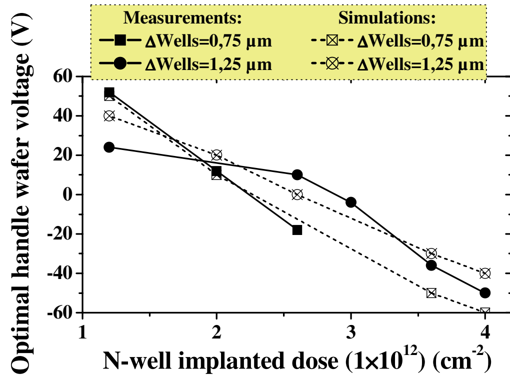

Figure 3. Optimal HWV in terms of V_{BR} as a function of the N-well implanted dose for different ΔWells values. (ΔPwell = 0.75 µm).

For large spacing between N- and P-well masks (ΔWells = 1.25µm), the HWV which gives the maximum breakdown voltage is less sensitive to the N-well implanted dose. The fast drop for ΔWells equal to 0.75 µm comes from the excessive N-well doping concentration at the Silicon surface, as it can be observed in figure 4. This is due to the fact that the same N-well profile is used for both the N-type LDD and channel definition in complementary power NMOS and PMOS, respectively due to process constraints which limits the number of masks.

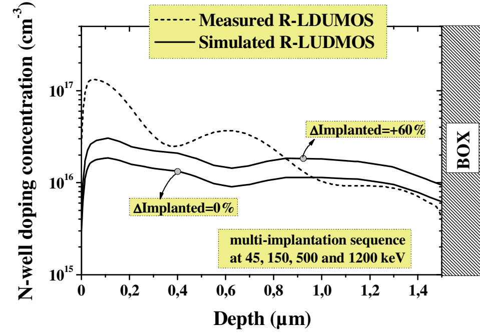

Figure 4. Phosphorus (N-well) doping profile throughout the SOI active layer after the multi-implantation sequence used in the measured R-LUDMOS and the proposed optimal R-LUDMOS.

This critical Phosphorus concentration peak at the Silicon surface is avoided for the case of ΔWells of 1.25 µm since the STI block act as a stopper. In order to explain this phenomenon, the electric field and the impact ionization values as a function of HWV at the three nodes (N1, N2 and N3) defined in figure 1 (a) are represented in figure 5.

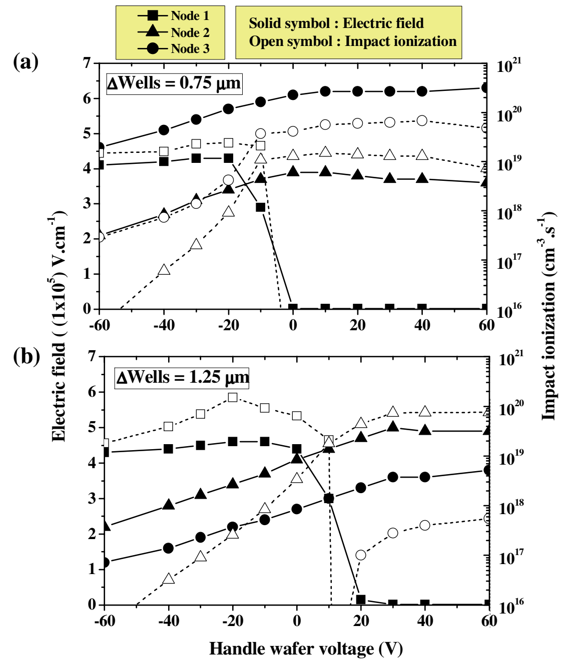

Figure 5. Electric field and impact ionization values as a function of HWV at the three deffined nodes for ΔPwell of 0.75µm, (a) ΔWells of 0.75 µm and (b) 1.25 µm.

A harmful electric field and a high avalanche generation at the node N3 are clearly observed for ΔWells equal to 0.75µm due to the previously commented high Phosphorus (N-well) concentration at channel/drift region surface, being obviously reduced for ΔWells of 1.25 µm.

III. STRUCTURE OPTIMIZATION

A. New N-well doping profile

In order to improve the voltage capability of the R-LUDMOS transistor, the reduction of the N-well doping concentration at the drift region surface is mandatory. Then, the N-well implantation sequence is re-defined, leading to an almost constant drift doping profile throughout the SOI Silicon active area, as observed in figure 4.

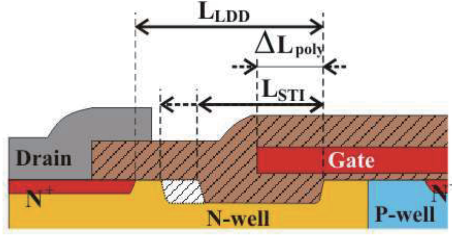

Figure 6. Schematic cross section detail of drift region with the L_{STI}, ΔL_{Poly} and L_{LDD} parameters.

B. $R_{on\text{-}sp}$ / V_{BR} trade-off

The R-LUDMOS with the new N-well doping profile previously defined is studied in terms of $R_{on\text{-}sp}/V_{BR}$ trade-off for different STI lengths (L_{STI}) and ΔWells values with a new L_{LDD} of 7 µm, as described in figure 6.

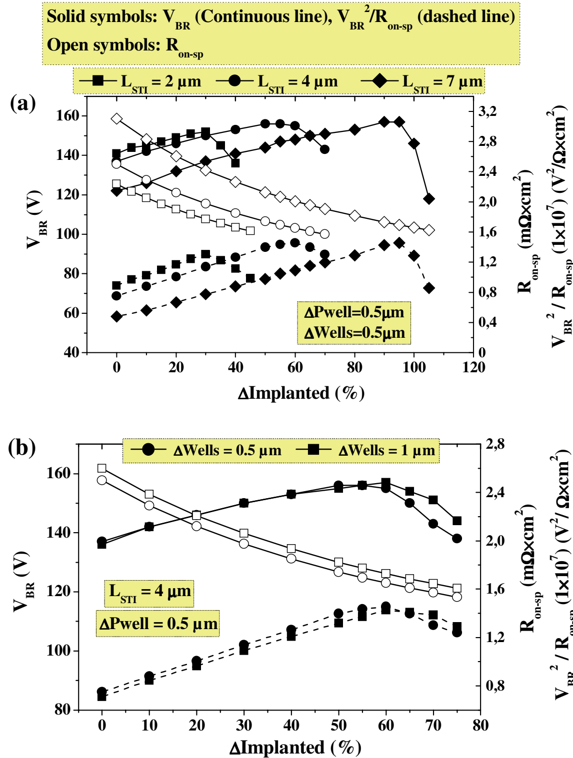

Figure 7. $R_{on\text{-}sp}/V_{BR}$ trade-off and FOM ($V_{BR}^2/R_{on\text{-}sp}$) as a function of N-well total implant dose given in figure 5 for different (a) L_{STI} and (b) ΔWells.

As seen from figure 7 (a), the longer the L_{STI} the higher the N-well optimal implant dose in terms of V_{BR}. In the case of an STI block covering entirely the LDD region (L_{STI} = 7 µm), the V_{BR} maximum value is followed by a quick fall down as the N-well doping concentration increases. This fast voltage capability degradation is related with the worse electric field distribution at breakdown, especially at the drain side STI corner. On the other hand, the transition of ΔWells from 0.5 to 1 µm (see figure 7 (b)) smoothes the P-well/N-well junction transition, but moves the junction closer to the STI border. As a result, a quick depletion of the N-well at the channel/drift region surface reduces the electric field in the P-well/N-well junction region, thus leading to a slightly less sensitive V_{BR} with the N-well implanted dose. In contrast, the shorter accumulation region length leads to worse current transition between channel and bulk, thus slightly increasing the $R_{on\text{-}sp}$.

C. V_{BR} vs HWV evolution

The V_{BR} variations versus HWV of the proposed R-LUDMOS are represented in figure 8 for different L_{STI}. The N-well implantation dose has been chosen in order to reach the maximum breakdown voltage at HWV close to 0V.

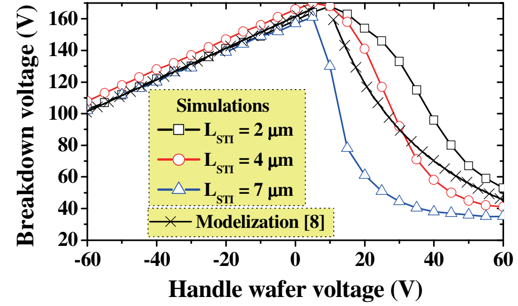

Figure 8. V_{BR} as a function of HWV for different L_{STI} values.

Results from figure 8 show more pronounced negative variations of V_{BR} evolution for positive HWV values as L_{STI} increases. When increasing HWV from 0 V to positive values, the breakdown localization moves from the N^+ drain diffusion to the drain and finally to the source side STI corners. In the case of an STI covering the whole LDD region, the N^+ drain diffusion and the drain STI border are merged, leading to a worse electric field distribution evolution in the LDD region which explains the fast V_{BR} degradation.

D. Safe Operating Area

Once determined the N-well optimal doping concentration for every LDMOS structure, the electrical SOA is compared in this section by analyzing the results of body current (I_{body}) [5]. The methodology sequence used in this study is explained in the example of figure 9. First, the body and drain currents as a function of drain voltage (V_D) of the optimal simulated R-LUDMOS in terms of $R_{on\text{-}sp}/V_{BR}$ trade-off are represented in figure 9 (a). This plot is performed in order to find the I_{body} which leads to snap-back conditions for each structure. Once extracted this value, simulations of I_{body} as a function of the gate voltage (V_G) are performed (see figure 9 (b)) at high stress conditions (V_D = 60 V) with the purpose of obtaining the maximum V_G which leads to the I_{body} at snap-back from figure 9 (a). The I_{body} peak appeared at low V_G values is also extracted from this simulation, as seen in figure 9 (c). This

high I_{body} increase at sub-threshold V_G values is related to the increase of the impact ionization at the channel/drift region surface. Optimal drift region designs should give both low I_{body} peak and high maximum V_G values in order to reach high on-state breakdown voltage and prevent the snap-back phenomenon at operative voltage. So, the values of maximum I_{body} and V_G extracted by means of the methodology reported in figure 9 are represented in figure 10 as a function of the N-well implanted dose for different L_{STI}, ΔPwell and ΔWells values.

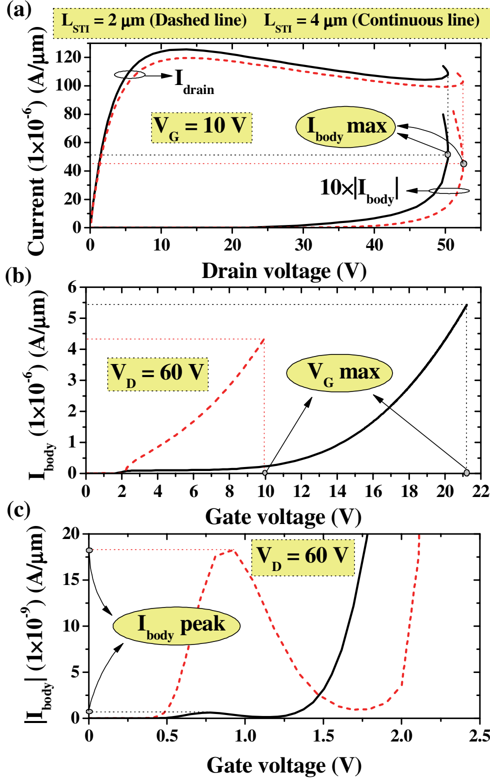

Figure 9. Simulation results of (a) I_D-V_D characteristic showing the electrical SOA boundary and (b, c) I_{body}-V_G characteristic for R-LUDMOS optimal transistors in terms of $R_{on\text{-}sp}/V_{BR}$ trade-off with L_{STI} of 2 and 4 µm.

Results from figure 10 show that the lowest achievable I_{body} peak is possible with the lowest values of ΔWells. Increasing the spacing between the N-well and P-well implantation masks will move the junction closer to the STI corner. Hence, the current transition path from channel to bulk moves closer to the STI corner where high electric field is expected, thus raising the impact ionization value. On the other hand, the L_{STI} increment reduces the I_{body} peak but also reduce the maximum V_G, thus showing a compromise between both parameters. Hence, optimal I_{body} peak/V_{Gmax} trade-off is possible for designs with L_{STI} of 4 µm, being the V_{Gmax} strongly penalized when the STI covers the whole drift region (L_{STI} of 7 µm).

IV. Conclusion

The voltage capability and electric SOA characteristics of high voltage (150V) R-LUDMOS structures based upon a 0.18µm CMOS technology on thin-SOI are analyzed by means of TCAD numerical simulations. The measures performed on R-LUDMOS transistors have shown a pronounced V_{BR} degradation as HWV increases due to the located high concentration of phosphorus (N-well) at the channel surface. The performances of the R-LUDMOS can be easily improved by using a different N-well doping profile for the drift region and the definition of an STI partially covering the LDD region. The best results in terms of $R_{on\text{-}sp}/V_{BR}$ and SOA are found for an STI length of 4 µm and spacing between N-well and P-well masks of 0.5 µm

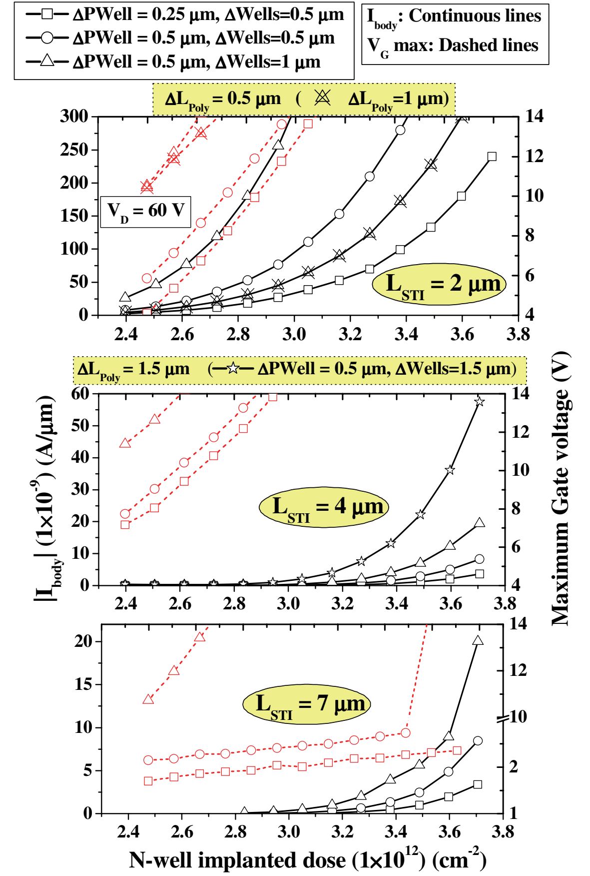

Figure 10. Electrical SOA simulations of I_{body} first peak value obtained from I_{body}-V_G characteristic at V_D = 60 V and maximum V_G value at SOA boundary conditions in R-LUDMOS transistors with L_{STI} of 2, 4 and 7 µm.

Acknowledgment

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References

[1] S Matsumoto et al. Jpn. J. Appl. Phys. 1995;34: 817 – 21.
[2] R Zhu et al. In Proc. ISPSD 2006, pp. 1 – 4.
[3] I Cortés et al. Semicond. Sci. Technol. 2008;23(8):095024.
[4] SH Chen et al. *Japan J. Appl. Phys* 2004;43:54 – 60.
[5] PL Hower et al. In Proc. ISPSD 1999, pp. 55 – 58.
[6] S Schwantes et al. In Proc. ESSDERC 2004, pp. 253 – 56.